



# STB20NM60A-1 STP20NM60A - STF20NM60A

N-CHANNEL 650V @  $T_{jmax}$  -  $0.25\Omega$  - 20A I<sup>2</sup>PAK/TO-220/TO-220FP  
MDmesh™ MOSFET

TYPE	V <sub>DSS</sub> @ T <sub>jmax</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STB20NM60A-1	650 V	< 0.29 $\Omega$	20 A
STP20NM60A	650 V	< 0.29 $\Omega$	20 A
STF20NM60A	650 V	< 0.29 $\Omega$	20 A

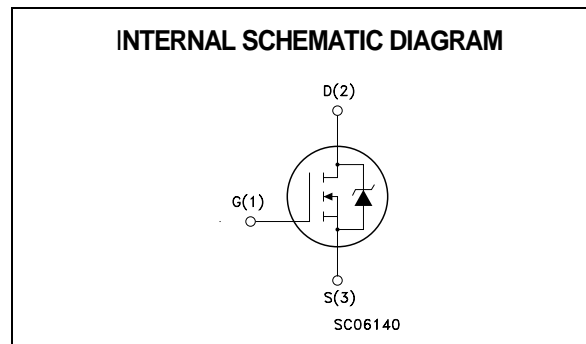
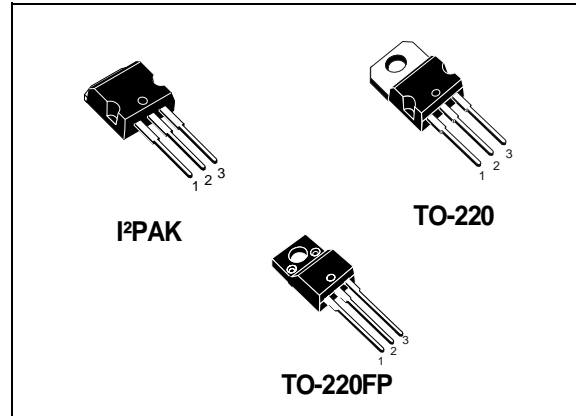
- TYPICAL R<sub>DS(on)</sub> = 0.25 $\Omega$
- HIGH dv/dt
- LOW INPUT CAPACITANCE AND GATE CHARGE
- LOW GATE INPUT RESISTANCE

## DESCRIPTION

The MDmesh™ is a new revolutionary MOSFET technology that associates the Multiple Drain process with the Company's PowerMESH™ horizontal layout. The resulting product has an outstanding low on-resistance, impressively high dv/dt and excellent avalanche characteristics. The adoption of the Company's proprietary strip technique yields overall dynamic performance that is significantly better than that of similar competition's products.

## APPLICATIONS

- SPECIFICALLY DESIGNED FOR ADAPTERS QUASI-RESONANT CONFIGURATION



## ORDERING INFORMATION

SALES TYPE	MARKING	PACKAGE	PACKAGING
STB20NM60A-1	B20NM60A	I <sup>2</sup> PAK	TUBE
STP20NM60A	P20NM60A	TO-220	TUBE
STF20NM60A	F20NM60A	TO-220FP	TUBE

## STB20NM60A-1/STP20NM60A/STF20NM60A

### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		STB20NM60A-1 STP20NM60A	STF20NM60A	
V <sub>GS</sub>	Gate-source Voltage	±30		V
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 25°C	20	20(*)	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 100°C	12.6	12.6(*)	A
I <sub>DM</sub> (•)	Drain Current (pulsed)	80	80(*)	A
P <sub>TOT</sub>	Total Dissipation at T <sub>C</sub> = 25°C	192	45	W
	Derating Factor	1.2	0.36	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	15		V/ns
V <sub>ISO</sub>	Insulation Withstand Voltage (DC)	--	2500	V
T <sub>stg</sub>	Storage Temperature	-55 to 150		°C
T <sub>j</sub>	Max. Operating Junction Temperature			

(•) Pulse width limited by safe operating area

(1) I<sub>SD</sub> ≤ 20A, di/dt ≤ 400 A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>j</sub> ≤ T<sub>JMAX</sub>.

(\*) Limited only by maximum temperature allowed

### THERMAL DATA

		I <sup>2</sup> PAK/TO-220	TO-220FP	
R <sub>thj-case</sub>	Thermal Resistance Junction-case Max	0.65	2.8	°C/W
R <sub>thj-amb</sub>	Thermal Resistance Junction-ambient Max	62.5		°C/W
T <sub>l</sub>	Maximum Lead Temperature For Soldering Purpose	300		°C

### ELECTRICAL CHARACTERISTICS (T<sub>CASE</sub> = 25 °C UNLESS OTHERWISE SPECIFIED)

ON/OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0	600			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max Rating V <sub>DS</sub> = Max Rating, T <sub>C</sub> = 125 °C			1 10	μA μA
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 30V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2	3	4	V
R <sub>DS(on)</sub>	Static Drain-source On Resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 10A		0.25	0.29	Ω

**ELECTRICAL CHARACTERISTICS (CONTINUED)**  
DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs}$ (1)	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ , $I_D = 10A$		11		S
$C_{iss}$	Input Capacitance	$V_{DS} = 25V$ , $f = 1$ MHz, $V_{GS} = 0$		1630		pF
$C_{oss}$	Output Capacitance			350		pF
$C_{rss}$	Reverse Transfer Capacitance			33		pF
$C_{oss\ eq.}$ (2)	Equivalent Output Capacitance	$V_{GS} = 0V$ , $V_{DS} = 0V$ to $400V$		150		pF

(1) Pulsed: Pulse duration = 300  $\mu$ s, duty cycle 1.5 %.

(2)  $C_{oss\ eq.}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 300V$ , $I_D = 10$ A $R_G = 4.7\Omega$ , $V_{GS} = 10V$ (see test circuit, Figure 3)		20		ns
$t_r$	Rise Time			16		ns
$Q_g$	Total Gate Charge	$V_{DD} = 400V$ , $I_D = 20A$ , $V_{GS} = 10V$		45	60	nC
$Q_{gs}$	Gate-Source Charge			8.2		nC
$Q_{gd}$	Gate-Drain Charge			19		nC

**SWITCHING OFF**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off Delay Time	$V_{DD} = 300V$ , $I_D = 20$ A, $R_G = 4.7\Omega$ , $V_{GS} = 10V$ (see test circuit, Figure 5)		46		ns
$t_f$	Fall Time			20		ns

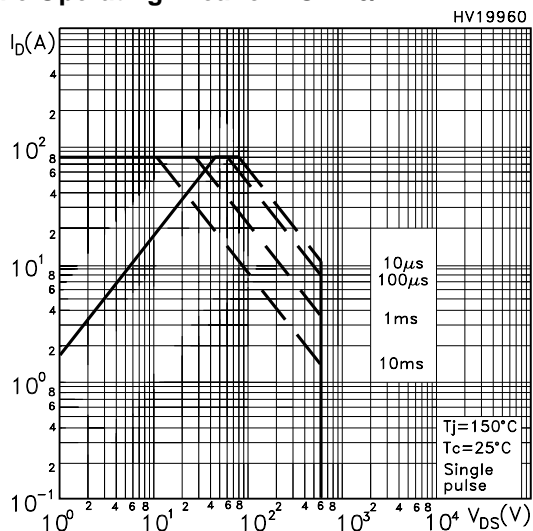
**SOURCE DRAIN DIODE**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain Current				20	A
$I_{SDM}$ (2)	Source-drain Current (pulsed)				80	A
$V_{SD}$ (1)	Forward On Voltage	$I_{SD} = 20$ A, $V_{GS} = 0$			1.5	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 20$ A, $di/dt = 100A/\mu$ s, $V_{DD} = 50$ V, $T_j = 25^\circ C$ (see test circuit, Figure 5)		432		ns
$Q_{rr}$	Reverse Recovery Charge			5.1		$\mu$ C
$I_{rrm}$	Reverse Recovery Current			23.6		A
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 20$ A, $di/dt = 100A/\mu$ s, $V_{DD} = 50$ V, $T_j = 150^\circ C$ (see test circuit, Figure 5)		595		ns
$Q_{rr}$	Reverse Recovery Charge			7.3		$\mu$ C
$I_{rrm}$	Reverse Recovery Current			24.8		A

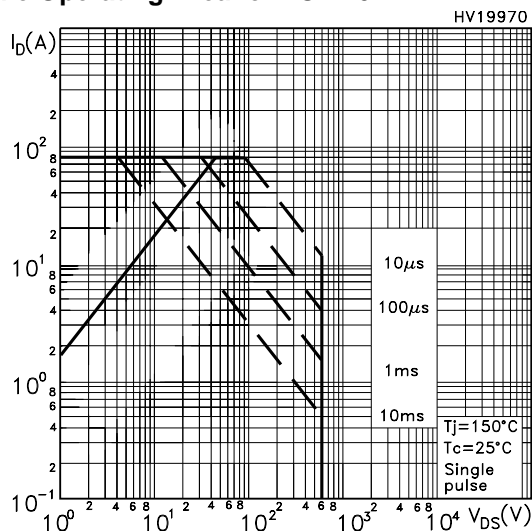
Note: 1. Pulsed: Pulse duration = 300  $\mu$ s, duty cycle 1.5 %.

2. Pulse width limited by safe operating area.

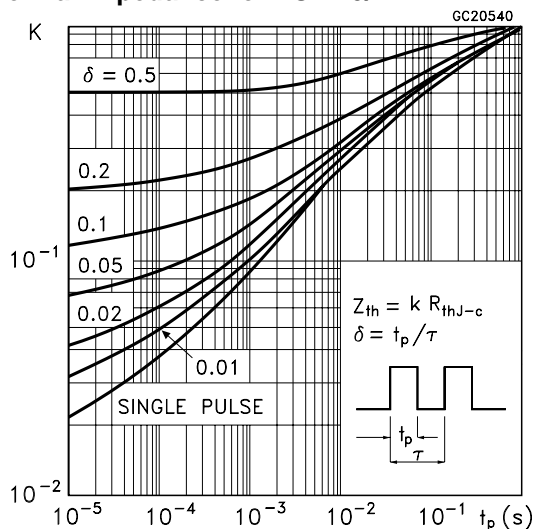
Safe Operating Area for TO-220/I2PAK



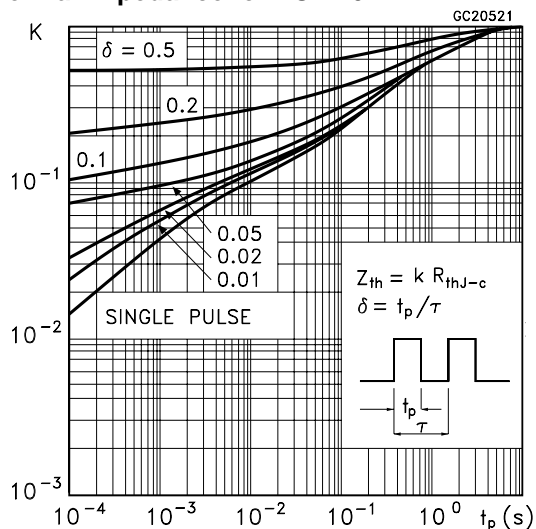
Safe Operating Area for TO-220FP



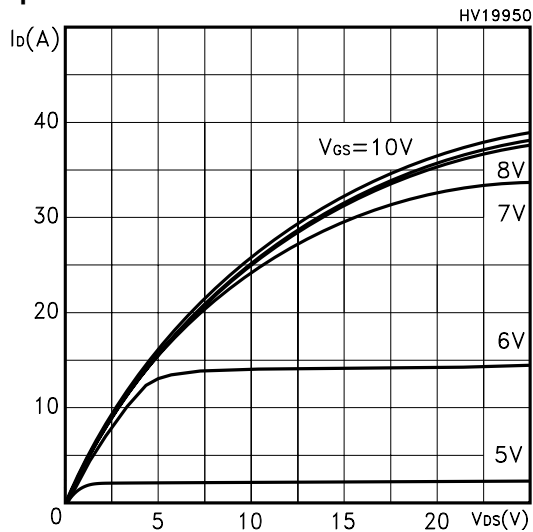
Thermal Impedance for TO-220/I2PAK



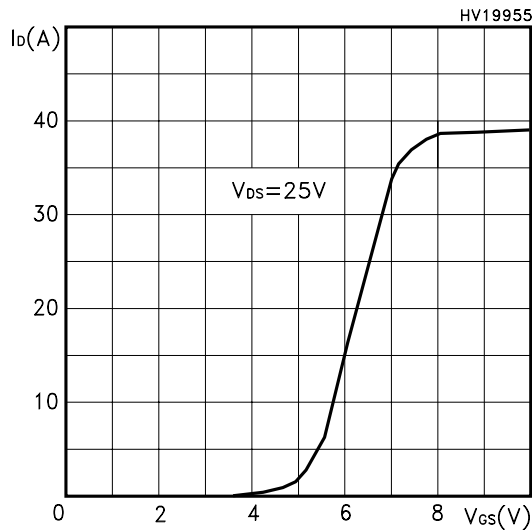
Thermal Impedance for TO-220FP



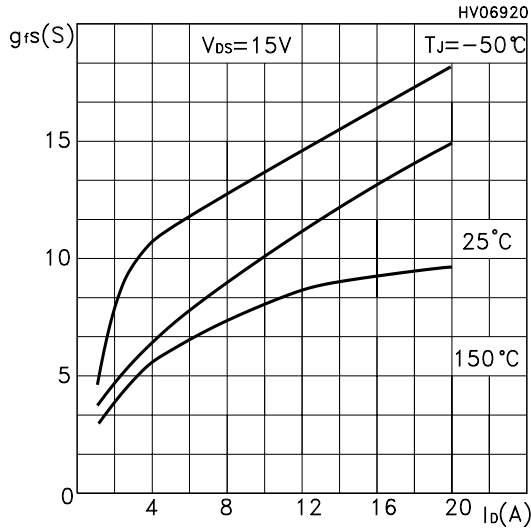
Output Characteristics



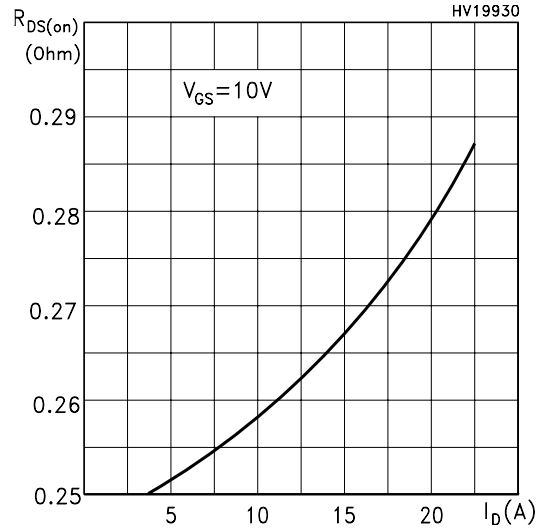
Transfer Characteristics



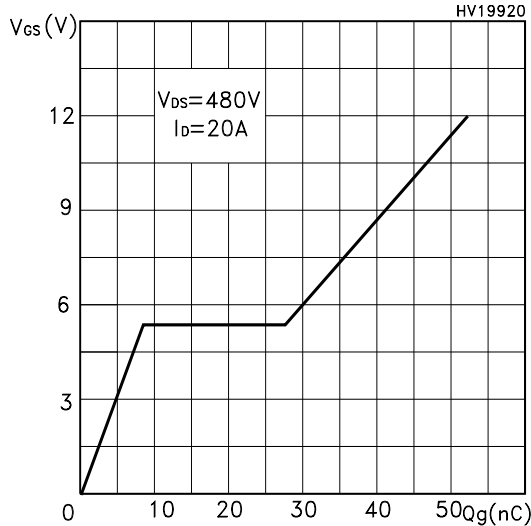
**Transconductance**



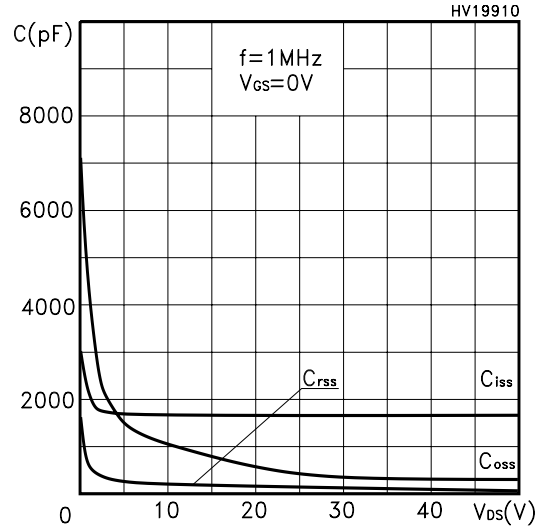
**Static Drain-Source On Resistance**



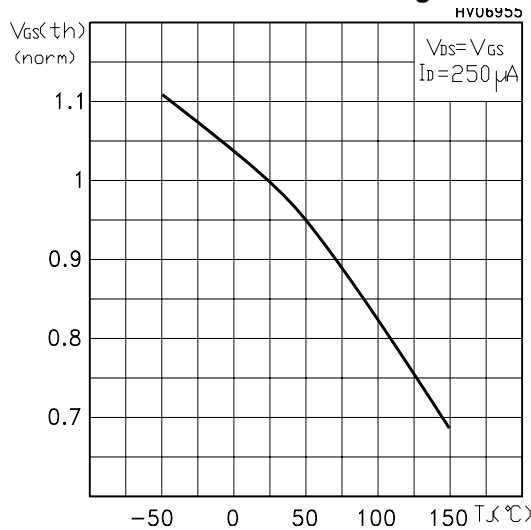
**Gate Charge vs Gate-source Voltage**



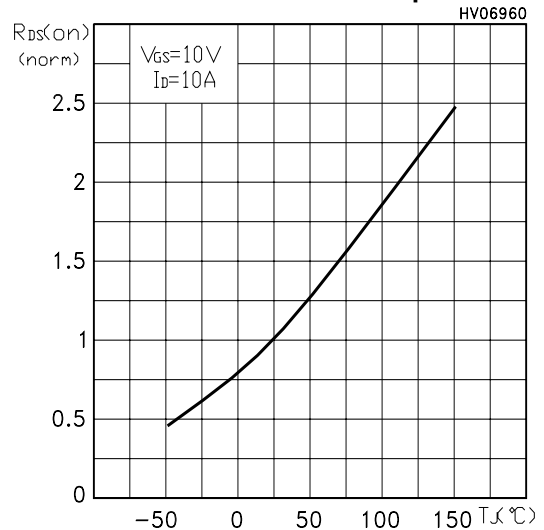
**Capacitance Variations**



**Normalized Gate Threshold Voltage vs Temp.**

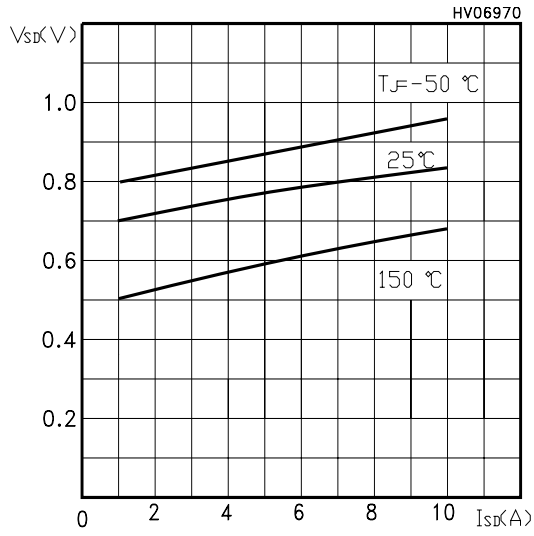


**Normalized On Resistance vs Temperature**

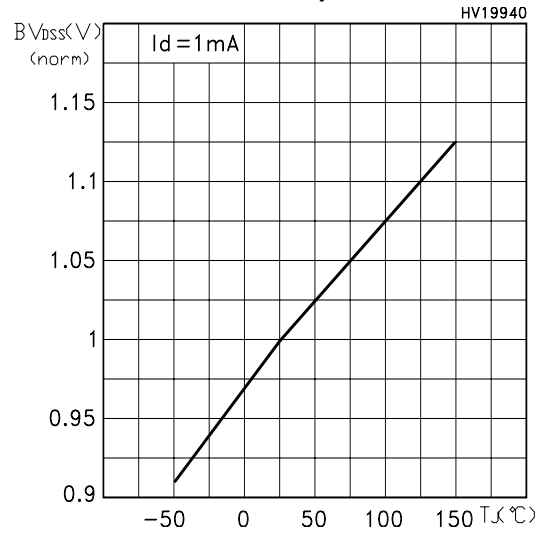


**STB20NM60A-1/STP20NM60A/STF20NM60A**

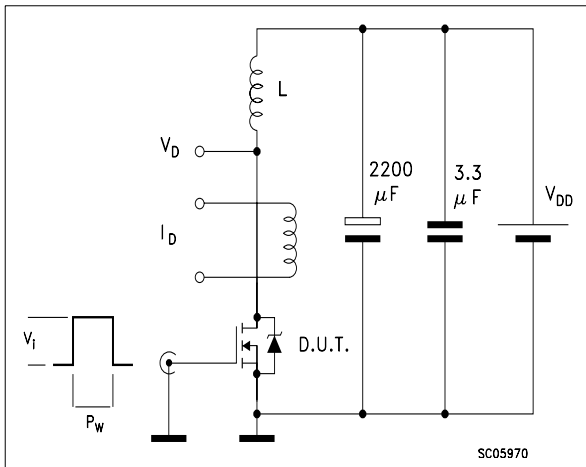
**Source-drain Diode Forward Characteristics**



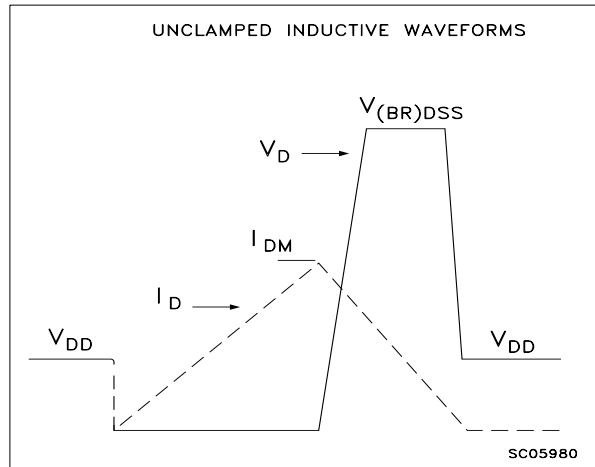
**Normalized BVDSS vs Temperature**



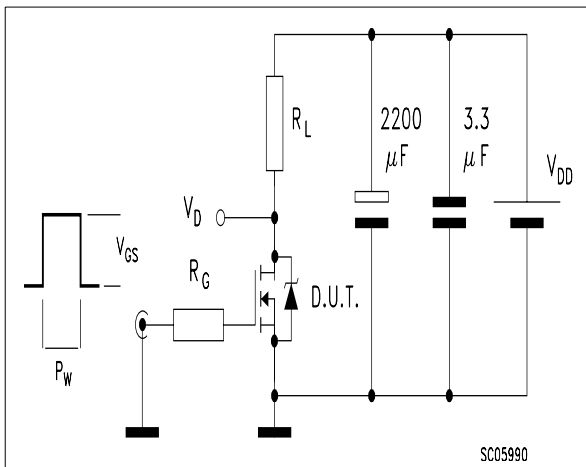
**Fig. 1: Unclamped Inductive Load Test Circuit**



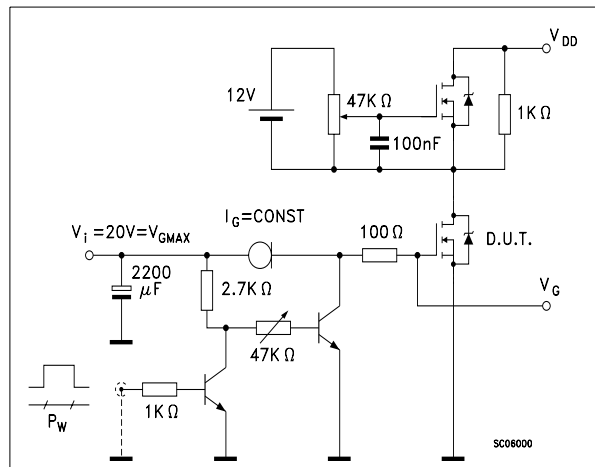
**Fig. 2: Unclamped Inductive Waveform**



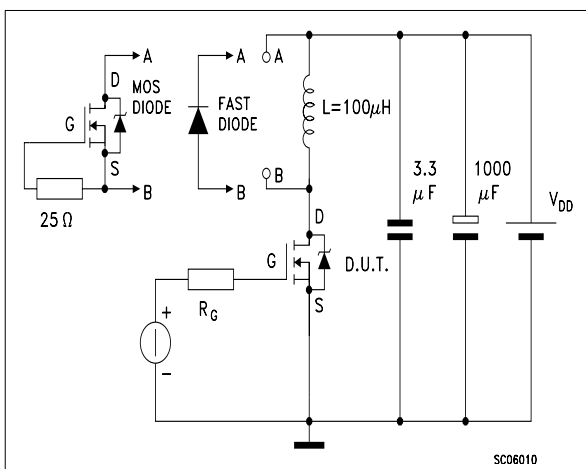
**Fig. 3: Switching Times Test Circuit For Resistive Load**



**Fig. 4: Gate Charge test Circuit**

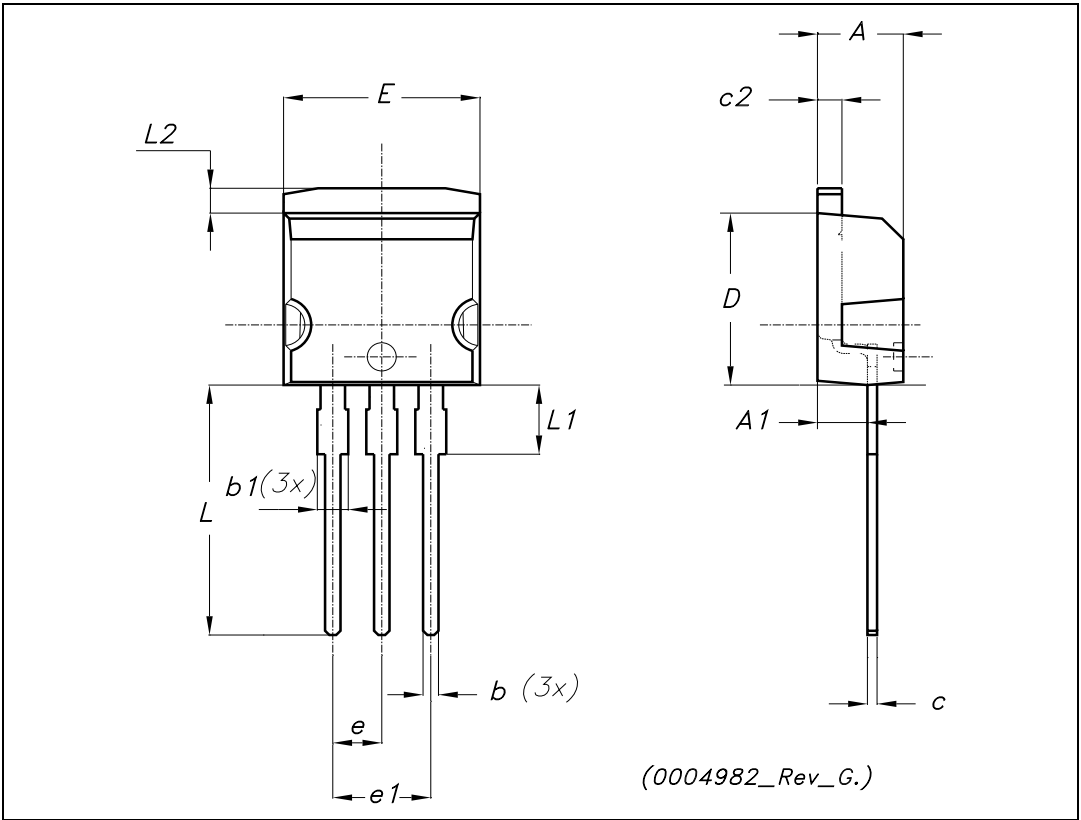


**Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times**



**TO-262 (I<sup>2</sup>PAK) MECHANICAL DATA**

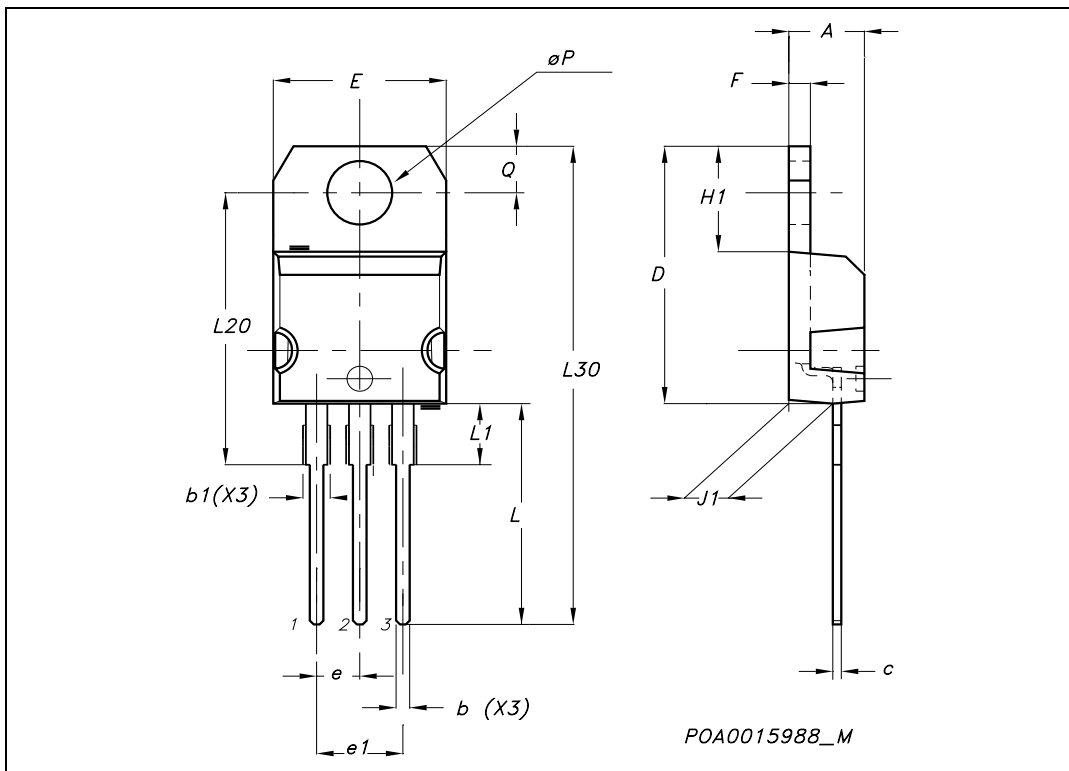
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
A1	2.40		2.72	0.094		0.107
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.49		0.70	0.019		0.027
c2	1.23		1.32	0.048		0.052
D	8.95		9.35	0.352		0.368
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
E	10		10.40	0.393		0.410
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L2	1.27		1.40	0.050		0.055





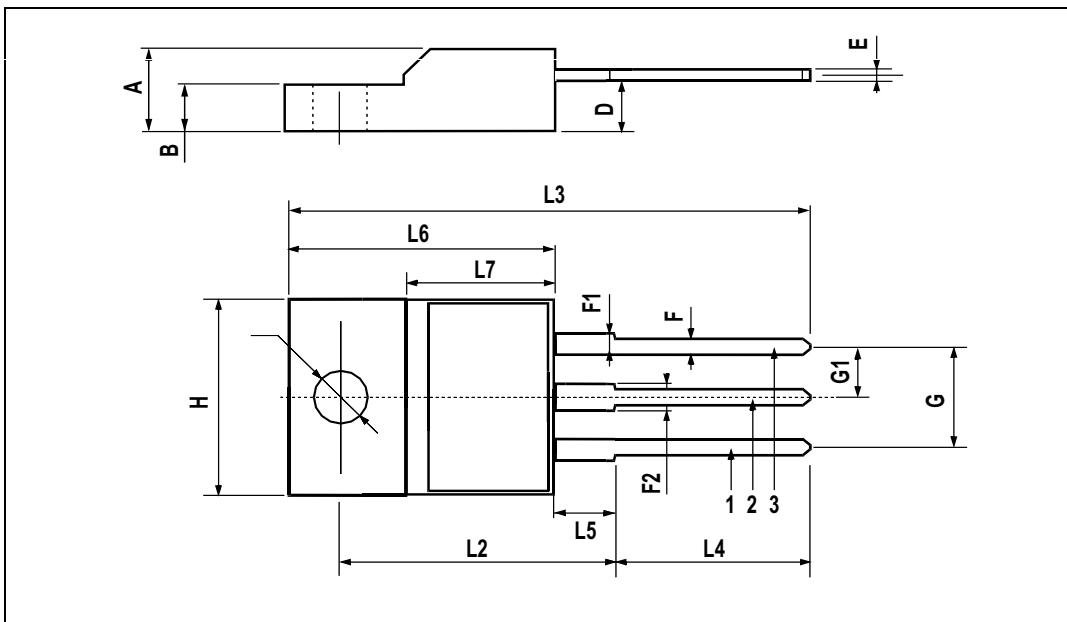
**TO-220 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



**TO-220FP MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



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